IN THE CLAIMS

Please amend the Claims as follows:

1. (currently amended) A method of copper metallization in the fabrication of an integrated circuit device comprising:

providing an opening through a dielectric layer overlying a substrate on a wafer;

forming a copper layer overlying said dielectric layer and completely filling said opening;

polishing back said copper layer to leave said copper layer only within said opening;

coating an oxide layer <u>on said dielectric layer and said copper layer and</u> on the walls of a deposition chamber;

thereafter heating said wafer in said deposition chamber using a plasma; and

thereafter depositing in said deposition chamber a capping layer overlying said oxide layer to complete said copper metallization in said fabrication of said integrated circuit device.

2. (original) The method according to Claim 1 further comprising forming semiconductor device structures in

and on said substrate wherein said semiconductor device structures include gate electrodes, source/drain regions, and lower level metallization.

3. (original) The method according to Claim 1 wherein said opening is made to a semiconductor device structure within said substrate.

4. (original) The method according to Claim 1 wherein said step of forming said copper layer is selected from the group consisting of: physical vapor deposition, chemical vapor deposition, electroplating, and electroless plating.

5. (original) The method according to Claim 1 wherein said step of polishing back said copper layer comprises chemical mechanical polishing.

6. (original) The method according to Claim 1 wherein said steps of coating said oxide layer, heating said wafer, and depositing said capping layer are performed in a single plasma-enhanced chemical vapor deposition chamber.

7. (original) The method according to Claim 1 wherein said oxide layer is coated to a thickness of between about 10 and 10,000 Angstroms.

8. (original) The method according to Claim 1 wherein said plasma comprises NH_3 plasma.

9. (original) The method according to Claim 1 wherein said step of heating said wafer comprises heating said wafer to between about 200 and 600 ^{o}C.

10. (original) The method according to Claim 1 wherein said capping layer is selected from the group consisting of silicon nitride and silicon carbide and wherein said capping layer has a thickness of between about 100 and 2000 Angstroms.

11. (original) The method according to Claim 1 wherein said the time elapsed between said step of polishing back said copper layer and said step of depositing said capping layer is less than one day (24 hours).

12. (previously presented) A method of copper metallization in the fabrication of an integrated circuit device comprising:

providing an opening through a dielectric layer overlying a substrate on a wafer;

forming a copper layer overlying said dielectric layer and completely filling said opening;

polishing back said copper layer to leave said copper layer only within said opening;

coating an oxide layer on said dielectric layer and said copper layer and on the walls of a deposition chamber;

thereafter heating said wafer in said deposition chamber using NH_3 plasma; and

thereafter depositing in said deposition chamber a capping layer overlying said oxide layer to complete said copper metallization in said fabrication of said integrated circuit device.

13. (original) The method according to Claim 12 further comprising forming semiconductor device structures in and on said substrate wherein said semiconductor device structures include gate electrodes, source/drain regions, and lower level metallization.

14. (original) The method according to Claim 12 wherein said opening is made to a semiconductor device structure within said substrate.

15. (original) The method according to Claim 12 wherein said step of forming said copper layer is selected from the group consisting of: physical vapor deposition, chemical vapor deposition, electroplating, and electroless plating.

16. (original) The method according to Claim 12 wherein said step of polishing back said copper layer comprises chemical mechanical polishing.

17. (original) The method according to Claim 12 wherein said steps of coating said oxide layer, heating said wafer, and depositing said capping layer are performed in a single plasma-enhanced chemical vapor deposition chamber.

18. (original) The method according to Claim 12 wherein said oxide layer is coated to a thickness of between about 10 and 10,000 Angstroms.

19. (original) The method according to Claim 12 wherein said step of heating said wafer comprises heating said wafer to between about 200 and 600 ^{o}C.

20. (original) The method according to Claim 12 wherein said capping layer is selected from the group consisting of silicon nitride and silicon carbide and wherein said capping layer has a thickness of between about 100 and 2000 Angstroms.

21. (original) The method according to Claim 12 wherein said the time elapsed between said step of polishing back said copper layer and said step of depositing said capping layer is less than one day (24 hours).

22. (previously presented) A method of copper metallization in the fabrication of an integrated circuit device comprising:

providing an opening through a dielectric layer overlying a substrate on a wafer;

forming a copper layer overlying said dielectric layer and completely filling said opening;

polishing back said copper layer to leave said copper layer only within said opening; and

within 24 hours after said polishing back said copper layer, completing the following steps:

coating an oxide layer on said dielectric layer and said copper layer and on the walls of a deposition chamber;

thereafter heating in said deposition chamber said wafer using NH_3 plasma; and

thereafter depositing in said deposition chamber a capping layer overlying said oxide layer wherein said oxide layer on said walls of said deposition chamber prevents said capping layer from coating said deposition chamber walls thereby preventing formation of copper hillocks to complete said copper metallization in said fabrication of said integrated circuit device.

23. (original) The method according to Claim 22 further comprising forming semiconductor device structures in and on said substrate wherein said semiconductor device structures include gate electrodes, source/drain regions, and lower level metallization.

24. (original) The method according to Claim 22 wherein said opening is made to a semiconductor device structure within said substrate.

25. (original) The method according to Claim 22 wherein said step of forming said copper layer is selected from the group consisting of: physical vapor deposition, chemical vapor deposition, electroplating, and

electroless plating.

26. (original) The method according to Claim 22 wherein said step of polishing back said copper layer comprises chemical mechanical polishing.

27. (original) The method according to Claim 22 wherein said steps of coating said oxide layer, heating said wafer, and depositing said capping layer are performed in a single plasma-enhanced chemical vapor deposition chamber.

28. (original) The method according to Claim 22 wherein said oxide layer is coated to a thickness of between about 10 and 10,000 Angstroms.

29. (original) The method according to Claim 22 wherein said step of heating said wafer comprises heating said wafer to between about 200 and 600 ^{o}C.